REMARKS

Applicants thank the Examiner for the thorough examination of the application.

Claims 1-19 are pending. Claims 1, 6, 11, 14, 15 and 18 are independent. Claims 6-18 are withdrawn from consideration.

Reconsideration of the present application is respectfully requested.

Drawings

Applicants have not received a Notice of Draftsperson's Patent Drawing Review, Form PTO-948, indicating whether the formal drawings have been approved by the Official Draftsperson. It is respectfully submitted that the drawings comply with USPTO requirements. Clarification with the next official communication is respectfully requested.

Rejection under 35 U.S.C. §103(a)

Claims 1-5 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,121,947 to Furuhashi et al. in view of U.S. Patent No. 5,874,937 to Kesatoshi and U.S. Patent No. 5,739,887 to Ueda et al., and further in view of U.S. Patent No. 5,532,935 to Ninomiya et al. Claim 19 is rejected under 35 U.S.C. §103(a) as being unpatentable over Furuhashi et al. in view of Kesatoshi, Ueda et al. and Ninomiya et al., and further in view of U.S. Patent No. 6,535,985 to Oshima et al. These rejections are respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

Independent claim 1 recites a combination of elements in a liquid crystal monitor drive apparatus for driving a liquid crystal panel, including "a scaler for scaling the definition and timing of the digital graphic data by adjusting the timing of the graphic data based on the clock signal and adjusting the horizontal and vertical synchronous signals from the connector to match with a timing of the liquid crystal panel" and "a timing controller arranged to drive the liquid crystal panel based on the scaled digital graphic data, the adjusted clock signal, and the adjusted horizontal and vertical synchronous signals from the scaler."

It is respectfully submitted that the combination of elements set forth in independent claim 1 is not disclosed or rendered obvious by the applied prior art of record, including Furuhashi et al., Kesatoshi, Ueda et al., Ninomiya et al. or Oshima et al.

As conceded on page 3 of the Office Action, Furuhashi et al. does not teach a scaler for timing of digital graphic data. The Office Action turns to Kesatoshi for this teaching. Kesatoshi discloses a video image scaling apparatus which includes a scaler 36 that expands or contracts a video image to make the resolution of a video signal coincident with a standard resolution of an LCD panel 40. The video scaler 36 receives a digital video signal DPC and a synchronizing signal SYNC from a personal computer 100. The synchronizing signal SYNC includes a horizontal

synchronizing signal HSYNC1 and a vertical synchronizing signal VSYNC1. A writing operation into a frame memory 34 is carried out synchronously with a dot clock signal DCK1 and the synchronizing signals HSYNC1 and VSYNC1. See FIGS. 1and 3, col. 3, lines 29-50 and col. 4, lines 27-46). Thus, Kesatoshi is directed to adjusting the resolution of the input video signal to be coincident with the resolution of the display device based on the dot clock signal DCK1 and the synchronizing signals HSYNC1 and VSYNC1. Nowhere does Kesatoshi discuss a scaler which adjusts the horizontal and vertical synchronous signals to match with a timing of the liquid crystal panel, or a timing controller which drives the liquid crystal panel based on scaled digital graphic data, and the adjusted clock, horizontal and vertical signals, as required by the present invention.

Therefore, Kesatoshi does not teach "a scaler for scaling the definition and timing of the digital graphic data by adjusting the timing of the graphic data based on the clock signal and adjusting the horizontal and vertical synchronous signals from the connector to match with a timing of the liquid crystal panel" and "a timing controller arranged to drive the liquid crystal panel based on the scaled digital graphic data, the adjusted clock signal, and the adjusted horizontal and vertical synchronous signals from the scaler," as recited in claim 1.

The Office Action relies on Ueda et al. for a teaching of combining electronic components into an integrated circuit, and relies on Ninomiya et al. for a teaching of a peripheral circuit coupled to an inverter. However, these references do not teach

or suggest the above-cited limitation of claim 1 and, therefore, fail to cure the deficiencies of Furuhashi et al. and Kesatoshi.

In rejecting claim 19, the Office Action relies on Oshima et al. for a teaching of a peripheral circuit operating with a frequency signal much lower than that of the clock signal. However, Oshima et al. does not teach or suggest the above-cited limitation of claim 1, incorporated in claim 19, and therefore fails to cure the deficiencies of Furuhashi et al., Kesatoshi, Ueda et al. and Ninomiya et al.

Therefore, the Examiner has failed to establish a *prima facie* case of obviousness, based on the all three of the required basic criteria of:

1. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the references;
2. There must be a reasonable expectation of success; and
3. The prior art must teach or suggest all of the claimed limitations.

In view of the foregoing, it is respectfully submitted that the applied prior art of record, including Furuhashi et al., Kesatoshi, Ueda et al., Ito, or Applicants' disclosed related art, fails to teach or suggest the combinations of elements set forth in independent claim 1.

It is believed that independent claim 1 is allowable. Since the remaining claims depend from these allowable independent claims, they are also allowable for at least the above reasons, as well as for the additional limitations provided

thereby. Thus, all claims are allowable. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §103(a) are respectfully requested.

CONCLUSION

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. It is believed that a full and complete response has been made to the outstanding Office Action, and that the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, she is invited to telephone James T. Eller, Jr. (Reg. No. 39,538) at (703) 205-8000.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or to credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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